# 103 四技部工讀實務實習

明志科技大學
MING CHI UNIVERSITY OF TECHNOLOGY

## 成果發表展示會

專業主題

# Display Port Re-driver & PICMG1.3 Back Plane Design

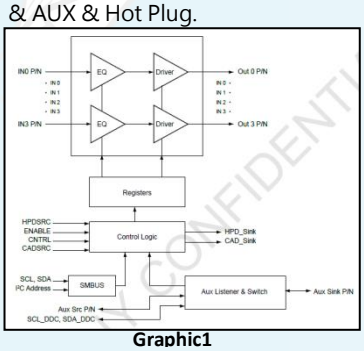
內容摘要

### Display Port Re-driver

- Display Port is a display signal of output Like VGA & HDMI. Because host signal can 't be pass, so we decide to Design a re-driver let it can be pass.
- Display Port composition of main link & AUX & Hot Plug.

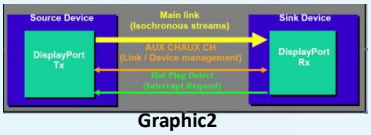

A101-1


A101-2



Graphic1

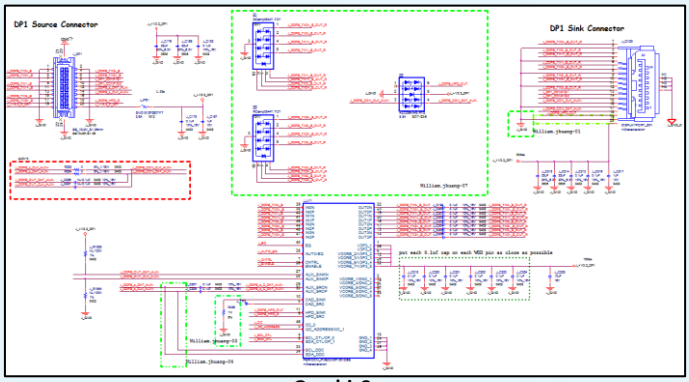
Enable have to Pull M or L , if pull H will into test mode. Others controller is control signal strength high or low.



Graphic2

Construction of Display port .

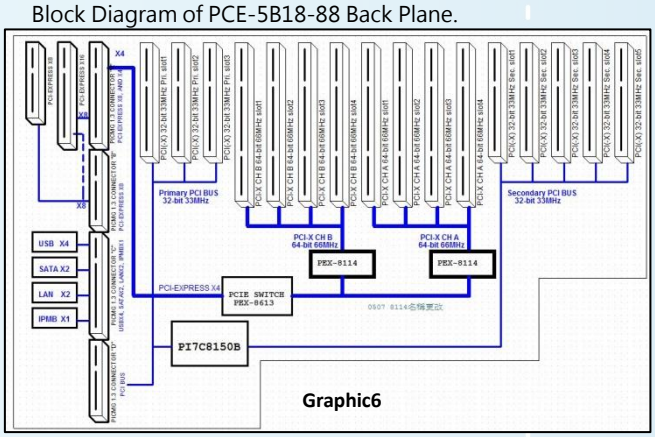
- We have to check the signal , function , Compatibility is ok before design the DP Re-driver circuit.
- The graphic3 is a Schematic of Display Port. The construction has a pin header, DP connector, ESD Parts & Re-driver.



Graphic3

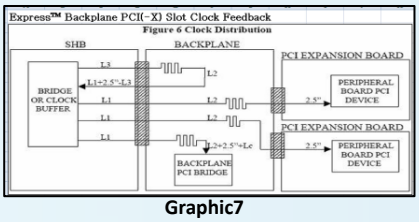
### PICMG1.3 Back Plane

- At first, custom want to use intel 6700 to design the back plane. Because Intel 6700 Bridge has Phase out and PLX-8114 performance is much better than other bridge, so we decide to replace Intel 6700.
- Block Diagram of PCE-5B18-88 Back Plane.



Graphic6

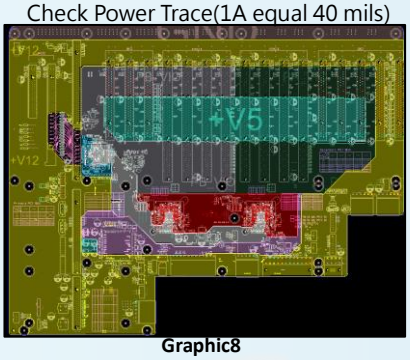
- Clock Feedback of PCI device Rule.



Graphic7

CLKA, CLKB, CLKC and CLKD between the slot and expansion slots shall be of the same length to minimize clock skew.

- Check Power Trace(1A equal 40 mils)


Graphic8

The power shapes have to over the default data, otherwise it power source will be not enough.

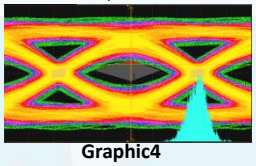
12 V → 41.9A ≒ 1680mils

3.3V → 42.5A ≒ 1720mils

5V → 40.8A ≒ 1632mils

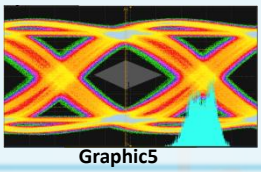
實習成果

- The Eye Diagram and Monitor compatibility were fail before use the DP Re-driver. Because the Pericom Chip Aux signal can't be work done , I use the TI Chip to design DP Circuit.

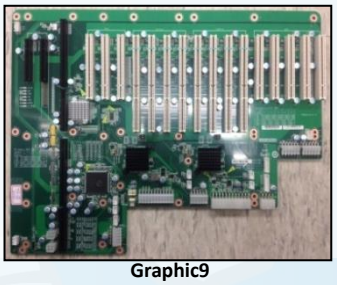

Graphic4

→Before use Re-driver eye Diagram.

After use Re-driver ← eye Diagram.


Graphic5

- This back plane have to change next version, Because have an issue of PLX-8114 3.3_PLX . PLX-8114 will leakage power from 3.3v to 3.3_PLX cause power sequence does not Meet spec. Solution is change terminal pull high resistance power from pcb layout.


Graphic9

- Summary:

During this year, I learned how to design back plane and IO board. It is difficult for me in the process, but I do it. And I obtained a lot of knowledge and skill that can't be known and learn from the school, it's a valuable experience.

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